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CLAIMS

[Claim(s)]
[Claim 1] The process which is the manufacture method of the semiconductor board which embeds in said semiconductor board and forms a layer of oxides by performing heat treatment after pouring in oxygen ion into a semiconductor board, and forms a porosity silicon layer in the surface of said semiconductor board, The process which forms a single crystal silicon layer on said porosity silicon layer, and after forming said single crystal silicon layer The manufacture method of the semiconductor board characterized by including the process which said porosity silicon layer is oxidized, embeds and forms a layer of oxides by heat-treating by pouring oxygen ion into a porosity silicon layer, and following it through said single crystal silicon layer.
[Claim 2] [form the ionic membrane-proof which has an opening partially on this single crystal silicon layer, pour in oxygen ion by using this ionic membrane-proof as a mask, and] by heat-treating continuously after forming a single crystal silicon layer on said porosity silicon layer The manufacture method of the semiconductor board according to claim 1 characterized by embedding in a semiconductor board and forming a layer of oxides alternatively.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture method of a semiconductor board of having an embedded oxide film inside.
[0002]
[Description of the Prior Art] In order to realize the three-dimensional structure for making the improvement in performance of a semiconductor device, and the densification of a device attain, it is silicon on insulator (Silicon On Insulator). Technology is to foundations. As this silicon-on-insulator technology, an insulating film is formed on a semiconductor board (silicon

wafer) with the method of growing silicon epitaxially on an insulating substrate (sapphire), and there is a method of growing up the single crystal of silicon on this insulating film.
[0003] There is the method of forming an insulating membrane layer (embedding oxide film layer) by injecting oxygen ion into a silicon substrate and making it heat-treat and react conventionally as technology which forms an insulating film on this silicon wafer.
[0004] Drawing 3 (a) With reference to - (c), the manufacture method of the conventional SOI substrate is explained in order of a process. First, the silicon substrate (silicon wafer) 1 as shown in drawing 3 (a) is prepared. And as shown in drawing 3 (b), oxygen ion 2 is poured into the field of the predetermined depth of this silicon substrate 1, and the oxygen-ion-implantation layer 3 is formed. The injection rate of the oxygen ion 2 sets 1018-/cm2 and the pouring depth to about 100nm, for example. Next, the embedded oxide film layer (silicon oxide film layer) 3a pinched between the silicon substrate 1 and the silicon layer 4 as shown in drawing 3 (c) is formed by heat-treating 1200-1350 degreeC, for example, and making oxygen and silicon by which ion implantation was carried out react.
[0005] [an above-mentioned method] by being called what is called a SIMOX (Separation by IMplantated OXygen) method, and repeating an ion implantation process and a heat treatment process by turns The crystallinity of the silicon layer 4 on the embedded oxide film layer 3a can be kept good.
[0006]
[Problem to be solved by the invention] However, by the conventional method, in a heat treatment process, an oxide film twice [about] the size of the volume of the silicon which reacted will be formed of the reaction of the oxygen and silicon by which ion implantation was carried out, therefore the silicon of the embedded oxide film layer 3a circumference will receive stress by it. Therefore, within the silicon substrate 1, the crystal defect was caused and there was a problem of leading to increase of junction leak etc.
[0007] Moreover, the demand which forms an embedded oxide film layer in a part of silicon substrate 1 alternatively as application of this SIMOX method may arise. For example, by forming an embedded oxide film layer only directly under [gate electrode] a transistor, it is strong to a short channel effect, and the element which has about the same S value as silicon on insulator can be formed. Or junction capacitance can be sharply reduced by forming an embedded oxide film layer only directly under the source region and a drain area. moreover, DRAM (Dynamic Random Access Memory) etc. -- by using silicon-on-insulator technology only for a memory cell part, junction leak of a cell transistor is reduced and it becomes possible to aim at an improvement of holding property.
[0008] Such a partial embedded oxide film layer can be formed by the method shown in drawing 4 (a) - (c). First, the silicon substrate 1 as shown in drawing 4 (a) is prepared, and as shown in drawing 4 (b), the resist layer 5 which has Opening 5a corresponding to an

embedded oxide film layer formation scheduled region is formed on the silicon substrate 1. Then, oxygen ion 2 is poured in by using this resist layer 5 as a mask, and two or more oxygen-ion-implantation layers 3 are alternatively formed in the field of the predetermined depth. Hereafter, after removing the resist layer 5, two or more embedded oxide film layers (silicon oxide film layer) 3a as shown in drawing 4 (c) can be formed by heat-treating and making oxygen and silicon by which ion implantation was carried out react like the above-mentioned method.

[0009] Although a partial embedded oxide film layer can be easily formed by such a method, also in this method, in the process which adds heat treatment, when silicon oxidizes, that volume becomes large, therefore the surrounding silicon of two or more embedded oxide film layers 3a will receive stress. Therefore, within the silicon substrate 1, the crystal defect was caused and there was a problem of leading to increase of junction leak etc. Furthermore, by this method, as shown in drawing 4 (c), the uneven part 6 arose on the surface of the silicon substrate 1, and there was a problem of interfering with device formation of a back process.

[0010] This invention was made in view of this problem, and [the technical problem] Even if it forms an embedded oxide film layer in a semiconductor board, it is in offering the manufacture method of the semiconductor board which sees on the whole, does not produce increase of the volume by oxidation reaction, and does not produce unevenness of the crystal defect by stress, or the surface.

[0011]

[Means for solving problem] Invention according to claim 1 is the manufacture method of the semiconductor board which embeds in said semiconductor board and forms a layer of oxides by performing heat treatment, after pouring in oxygen ion into a semiconductor board. The process which forms a porosity silicon layer in the surface of said semiconductor board, and the process which forms a single crystal silicon layer on said porosity silicon layer, After forming said single crystal silicon layer, the process which said porosity silicon layer is oxidized, embeds and forms a layer of oxides is included by heat-treating by pouring oxygen ion into a porosity silicon layer, and following it through said single crystal silicon layer.

[0012] After invention according to claim 2 forms a single crystal silicon layer on said porosity silicon layer in the manufacture method according to claim 1, The ionic membrane-proof which has an opening partially is formed on this single crystal silicon layer, oxygen ion is poured in by using this ionic membrane-proof as a mask, by heat-treating continuously, it embeds in a semiconductor board and a layer of oxides is formed alternatively.

[0013] A porosity silicon layer is formed in the surface of a semiconductor board by the manufacture method of the semiconductor board of this invention. Since pouring and heat treatment of oxygen ion which let a single crystal silicon layer pass are performed and an embedding layer of oxides is formed, after forming a single crystal silicon layer on this porosity

silicon layer In a heat treatment process, the volume integral which increased by oxidation reaction of porosity silicon is spent in the space in porosity silicon.

[0014]

[Mode for carrying out the invention] The form of operation of this invention is hereafter explained with reference to Drawings.

[0015] The form [0016] of the 1st operation Drawing 1 (a) - (e) expresses the manufacturing process of the semiconductor board concerning the form of operation of the 1st of this invention. First, as shown in drawing 1 (a), the semiconductor board 11 of a P type, for example, a silicon substrate, (silicon wafer) is prepared. And as shown in drawing 1 (b), the silicon substrate 11 in the mixed solution of HF(50wt%):C2 H5 OH(99.5%) =1:1, for example on condition of current density 10 - 80 mA/cm2 By carrying out anodization, the porosity silicon layer 12 of desired thickness (100nm-) is formed in the surface of the silicon substrate 11.

[0017] Next, as shown in drawing 1 (c), on the porosity silicon layer 12, silicon is grown epitaxially and thickness forms the about 100nm single crystal silicon layer 13, for example. Then, as shown in drawing 1 (d), the oxygen ion 14 is poured in through this single crystal silicon layer 13, and the oxygen-ion-implantation layer 15 is formed in the porosity silicon layer 12 in the silicon substrate 11. In addition, by this method, since change of the below-mentioned volume decreases most, the case where the volume ratio of silicon and oxygen is set to 1:2 needs to optimize the amount of ion implantation of oxygen so that it may become this ratio. Here, it is the amount of ion implantation 1018-/cm2 What is necessary is just to consider it as an order.

[0018] Next, as shown in drawing 1 (e), the embedded oxide film layer (silicon oxide film layer) 16 is formed in the silicon substrate 11 by heat-treating temperature 1200 - a 1350 degreeC grade, and making oxygen and silicon which were poured in into the oxygen-ion-implantation layer 15 react. By repeating such an ion implantation process and a heat treatment process by turns, the crystallinity of the single crystal silicon layer 13 on the embedded oxide film layer 16 can be kept good.

[0019] Thus, the porosity silicon layer 12 is formed in the surface of the silicon substrate 11 with the form of this operation. Since pouring and heat treatment of oxygen ion are performed and the embedded oxide film layer 16 was formed after forming the single crystal silicon layer 13 on this porosity silicon layer 12, the volume integral of the silicon which increased by oxidation reaction is spent in the space in the porosity silicon layer 12. For this reason, it is lost that see on the whole, volume does not increase by oxidation reaction around the embedded oxide film 16, and stress arises to surrounding silicon. Therefore, a crystal defect is caused like before and it is lost that junction leak increases. Moreover, by the method of depending on the form of this operation, since the oxidation rate of porosity silicon is quick compared with the conventional method, while heat treatment time is shortened, low temperature-ization of heat

treatment temperature can be attained.
[0020] The form [0021] of the 2nd operation Next, drawing 2 (a) - (e) explains the form of operation of the 2nd of this invention.
[0022] First, as shown in drawing 2 (a), the semiconductor board 21 of a P type, for example, a silicon substrate, (silicon wafer) is prepared. And as shown in drawing 2 (b), it is [be / for example, / it / under / mixed solution / of HF(50wt%):C2 H5 OH(99.5%) =1:1 / setting] the silicon substrate 21 Current density 10-80mA/cm2 [conditions] By carrying out anodization, the porosity silicon layer 22 of desired thickness (100nm-) is formed in the surface of the silicon substrate 21. Then, as shown in drawing 2 (c), on the porosity silicon layer 22, silicon is grown epitaxially and thickness forms the about 100nm single crystal silicon layer 23, for example. The process so far is the same as the process of drawing 1 (a) - (c).
[0023] With the form of this operation next, as shown in drawing 2 (d), the resist layer 24 which has Opening 24a corresponding to an embedded oxide film layer formation scheduled region is formed on the silicon substrate 21. Then, this resist layer 24 is used as a mask, oxygen ion 25 is poured in through the single crystal silicon layer 23, and two or more oxygen-ion-implantation layers 26 are alternatively formed in the porosity silicon layer 12.
[0024] Next, by heat-treating temperature 1200 - a 1350 degreeC grade, and making oxygen and silicon which were poured in into the oxygen-ion-implantation layer 26 react, after removing the resist layer 24, as shown in drawing 2 (e) Two or more embedded oxide film layers (silicon oxide film layer) 27 are alternatively formed in the silicon substrate 11. Also in this method, the crystallinity of the single crystal silicon layer 23 on the embedded oxide film layer 27 can be kept good by repeating an ion implantation process and a heat treatment process by turns.
[0025] Thus, the porosity silicon layer 22 is formed in the surface of the silicon substrate 21 with the form of this operation. Since two or more embedded oxide film layers 27 were formed by pouring in oxygen ion alternatively and performing that stress relief heat treatment after forming the single crystal silicon layer 23 on this porosity silicon layer 22 The volume integral of the silicon which increased by oxidation reaction as well as the form of the 1st operation is spent in the space in the porosity silicon layer 22. for this reason -- seeing on the whole -- two or more embedded oxide films 27 -- it is lost that the volume increase by oxidation reaction does not arise around each, and stress arises to surrounding silicon. Moreover, compared with the conventional method, since the oxidation rate of porosity silicon is quick, while heat treatment time is shortened, low temperature-ization of heat treatment temperature can be attained.
[0026] Moreover, with the form of this operation, it is lost that an uneven part arises of the surface of the silicon substrate 21 like [as shown in drawing 2 (e), it is flat, and] before. Therefore, the element of formation of the transistor with which the fault of both silicon on

insulator by the partial embedded oxide film 27 and bulk was compensated, or silicon on insulator and bulk mixed loading can be formed.

[0027] In addition, although explained using the silicon substrates 11 and 21 of a P type as a semiconductor board, you may make it use the semiconductor board of an N type in the form of the above-mentioned implementation. However, since a hole (electron hole) is needed in order to form a porosity silicone film by an anodization method, in using the semiconductor board of an N type, the means of supplying a hole, for example by optical irradiation is needed.

[0028]

[Effect of the Invention] [according to the manufacture method of a semiconductor board according to claim 1] as explained above After forming a porosity silicon layer in the surface of a semiconductor board and forming a silicon layer on this porosity silicon layer further Since it embeds by performing pouring and heat treatment of oxygen ion which let a silicon layer pass and the layer of oxides was formed, it is lost that stress starts the crystal of the embedded oxide film layer circumference of a semiconductor board. Therefore, what spoils the crystallinity of a semiconductor board is lost and increase of junction leak etc. can be prevented.

[0029] Moreover, according to the manufacture method of a semiconductor board according to claim 2, a silicon layer is formed on a porosity silicon layer. By using this ionic membrane-proof as a mask, pouring in oxygen ion through a silicon layer, and heat-treating continuously, after forming the ionic membrane-proof which has an opening partially on this silicon layer Since two or more embedding layers of oxides were formed alternatively, while what spoils the crystallinity of a semiconductor board is lost and being able to prevent increase of junction leak etc., a possibility that a concavo-convex part may occur on the surface of a substrate is lost, and trouble is lost in the device formation process of a back process.

[Translation done.]

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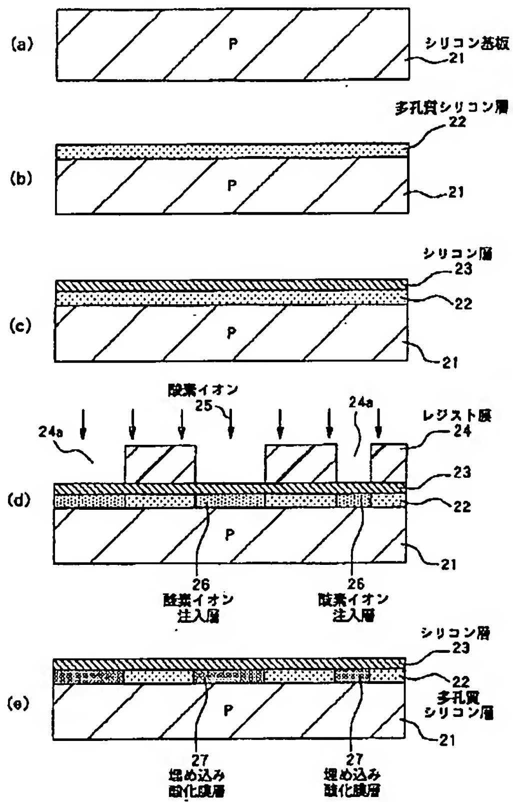
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a sectional view for explaining the manufacturing process by the form of operation of the 1st of this invention.
[Drawing 2] It is a sectional view for explaining the manufacturing process by the form of operation of the 2nd of this invention.
[Drawing 3] It is a sectional view for explaining the manufacturing process of a conventional method.
[Drawing 4] It is a sectional view for explaining other manufacturing processes of a conventional method.
[Explanations of letters or numerals]
11, 21 Semiconductor board
12, 22 Porosity silicon layer
13, 23 Silicon layer (epitaxial layer)
14, 25 Oxygen ion
15, 26 Oxygen-ion-implantation layer
16, 27 Embedded oxide film layer
24 Resist Layer (Ionic Membrane-proof)

[Translation done.]

Drawing selection Representative drawing



[Translation done.]